IN THE CLAIMS

1. (Currently Amended) A processing system comprising:
first and second processors; and
a non-volatile memory coupled to the first and second processors, the non-volatile memory comprises,
an array of non-volatile memory cells arranged in a plurality of addressable banks,
a data latch coupled to the array to store write data, and
read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the first processor to a first one of the plurality of addressable banks and simultaneously reads two or more second data from a second one of the plurality of addressable banks and provides the two or more second data to the second processor.

2. (Currently Amended) A method of operating a non-volatile memory device comprising:
receiving first data from a first external processor coupled to the memory;
storing the first data in a write latch;
writing the first data from the write latch to a first location in a memory array of the non-volatile memory device;
substantially simultaneously reading two or more second data from one or more remaining second locations ~~a second location~~ in the memory array of the non-volatile memory device; and
outputting the two or more second data to a second external processor coupled to the memory device.

3. (Currently Amended) The method of claim 2 wherein the first and second locations are a first addressable block and one or more second ~~first and second~~ addressable blocks of the memory array.

4. (original) The method of claim 3 wherein the first data is written to a row of the first block and the second data is read from a common row of the second block.

5. (Currently Amended) A non-volatile memory comprising:
an array of non-volatile memory cells arranged in a plurality of addressable banks; and
read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads two or more second data from a second one of the plurality of addressable banks, wherein the read/write circuitry receives the first data from a first external processor and provides the two or more second data to a second external processor.

6. (original) The non-volatile memory of claim 5 wherein the read/write circuitry comprises a write latch to store the first data.

7. (Currently Amended) The non-volatile memory of claim 5 wherein the plurality of addressable banks comprise four banks ~~blocks~~.

8. (Currently Amended) The non-volatile memory of claim 5 wherein the read/write circuitry writes the first data to an array row of the first one of the plurality of addressable banks and simultaneously reads the two or more second data from an array ~~the array~~ row of the second one of the plurality of addressable banks.

9. (original) The non-volatile memory of claim 5 wherein the non-volatile memory is a synchronous non-volatile memory.

10. (Currently Amended) A method of operating a non-volatile memory comprising:
providing first data to the non-volatile memory from a first external processor;
writing the first data to a first bank location in a memory array of the non-volatile memory;
substantially simultaneously reading two or more second data from a second bank location in the memory array of the non-volatile memory; and
outputting the two or more second data to a second external processor.

11. (original) The method of claim 10 further comprising accessing a common addressable row of the first and second bank locations prior to writing the first data and reading the two or more second data.

12. (new) The method of claim 10 further comprising storing the first data in a write latch.

13. (new) The processing system of claim 1 wherein the read/write circuitry further comprises a write latch to store the first data.

14. (new) The processing system of claim 1 wherein the plurality of addressable banks comprise four banks.

15. (new) The processing system of claim 1 wherein the non-volatile memory is a synchronous non-volatile memory.